driving, with a driving signal, a first switchably conductive device characterized by a first threshold voltage and connected between said node and a voltage source, said first switchably conductive device responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said first threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said first threshold voltage;

driving, with said driving signal, a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage and connected between said node and said voltage source, said second switchably conductive device responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said second threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said second threshold voltage.

REMARKS

Claims 1-11 are pending in the application and are presented for reconsideration. Claims 6 and 7 have been amended. Claims 1-5 and 8-11 remain in the application unchanged. An annotated version of the amendments is attached hereto for the Examiner's review.

Claim Rejections

Claims 1, 3-4, and 7-8 are rejected under 35 U.S.C. § 102(b), as being anticipated by US Patent No. 5,568,062 to Kaplinsky. Claims 10-11 are rejected under 35 U.S.C. § 102(b), as being anticipated by US Patent No. 5,877,647 to Vajapey et al.

Claims 2, 5-6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,568,062 to Kaplinsky in view of US Patent No. 5,877,647 to Vajapey et al.

Drawings

The drawings are objected to because:

In FIG. 1A, the decision boxes 14 and 18 are not complete, i.e., they do not have YES and NO paths. FIG. 1A has been amended to include the YES and NO paths.

In FIG. 1B, the decision boxes 34 and 38 are not complete, i.e., they do not have YES and NO paths. FIG. 1B has been amended to include the YES and NO paths.

In FIG. 4, the symbol 210 used to indicate an inverter is not a conventional symbol. FIG. 4 has been amended to use a conventional inverter symbol for the inverter 210.

Claim Objections

Claims 6 and 7 are objected to because of the following informalities:

As per claim 6, "3" recited on line 1 should be changed to --5--. The word "comprise" on line 4 should be changed to --comprises-- since its subject, i.e., the term "each", is singular. The word "transistors" recited on line 4 should be changed to --transistor--.

As per claim 7, "an" recited on line 14 should be changed to --and--.

Claims 6 and 7 have each been amended to make the above corrections.

I. Rejections of Claims Under 35 U.S.C. § 102

1. Legal standard for Rejecting Claims Under 35 U.S.C. §102

Under 35 U.S.C. § 102, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently

described, in a single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628 (Fed. Cir.), *cert. denied*, 484 U.S. 827 (1987). The mere absence from a reference of an explicit requirement of the claim cannot reasonably construed as an affirmative statement that the requirement is in the reference. *In re Evanega*, 829 F.2d 1110, 4 USPQ2d 1249 (Fed. Cir. 1987).

2. Response to 35 U.S.C. § 102 Rejections

a. Claims 1-4, 7-8

Claim 3 recites:

> 3. An apparatus for reducing the slew rate of transition edges of a digital signal on a node of an integrated circuit, comprising:
>
> a first switchably conductive device characterized by a first threshold voltage, said first switchably conductive device connected between said node and a voltage source and having a first switch responsive to a driving signal to allow current conduction from said voltage source to said node when said driving signal is substantially equal to or greater than said first threshold voltage and to disallow said current conduction when said driving signal is less than said first threshold voltage; and
>
> a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage, said second switchably conductive device connected between said node and said voltage source and having a second switch responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is substantially equal to or greater than said second threshold voltage and to disallow said current conduction when said driving signal is less than said second threshold voltage.

The Examiner cites Kaplinsky in rejecting Claims 1, 3-4, and 7-8 under 35 U.S.C. § 102(b). With regards to claim 3, the Examiner states that Kaplinsky discloses an apparatus (FIG. 10) for reducing the slew rate of transition edges of a digital signal (the signal OUTPUT at the node terminal 20) on a node (20) of an integrated circuit, comprising: a first switchably

conductive device (17) characterized by a first threshold voltage (the threshold voltage of transistor 17) wherein the first switchably conductive device (17) connected between the node (20) and a voltage source (VSS) and responsive to a driving signal (INPUT), and a second switchably conductive device (15) characterized by a second threshold voltage (the threshold voltage of transistor (15)) which greater than the first threshold voltage, wherein the second switchably conductive device (15) connected between the node (20) and the voltage source (VSS) and responsive to the driving signal (INPUT).

The Applicant respectfully traverses the Examiner's characterization of what Kaplinsky fairly teaches. The Examiner seeks to equate Kaplinsky's transistor 15 with Applicant's 126, and Kaplinsky's transistor 17 with Applicant's 144. The Examiner states that transistor 15 has a greater threshold voltage than the threshold voltage of transistor 17 because "the width of transistor 15 is 120 and transistor 17 is 680 and the lengths are the same", citing Kaplinsky, column 5, lines 5-6.

However, Kaplinsky does not teach or suggest that the threshold voltages of the two transistors 15 and 17 are actually different from one another. As known in the art, there are many parameters that go into the determination of the threshold voltage of a CMOS transistor. The Applicant hereby submits an additional reference, Pierret, Robert F., "Volume IV: Field Effect Devices", Modular Series On Solid State Devices, Addison-Wesley Publishing Company (1983), paragraph. 93-98. As described in Pierret, the threshold voltage of the CMOS transistor is determined by the gate oxide thickness, the substrate doping concentration, the substrate surface orientation, the material used in forming the gate, ion implantation concentration, etc. Pierret, a well-respected authority in the area of semiconductor devices, dedicates an entire section in his book to "threshold considerations". In this section (5.3, p. 93-98), Pierret outlines various

techniques used to adjust the threshold voltage of a MOS device, including varying the oxide thickness, varying the substrate doping concentration, changing the orientation of the substrate, changing the material used in forming the MOS gate, varying the ion implantation, and reverse biasing the bulk of the transistor relative to the source. Significantly, Pierret mentions nothing about varying the widths of the gate terminal while fixing the length of the gate terminal.

In addition, the threshold voltage of transistor 15 having dimensions 120/.8 and transistor 17 having dimensions 680/.8 may be identical depending on how the transistors are actually implemented. For example, the FETs 15 and 17 can be laid out with the same W/L. To wit, if in fabrication, the circuit is implemented using only 20/.8 FETs, transistor 15 may be fabricated using 6 20/.8 FETs in parallel while transistor 17 may be fabricated using 34 20/.8 FETs, the threshold voltage V_T will be the same for both transistors 15 and 17.

Importantly, nowhere in the Kaplinsky reference is there mention that the actual threshold voltages of the two transistors 15 and 17 are actually different. Accordingly, per *In re Evanega*, the mere absence from the Kaplinsky reference of the explicit requirement of claim 3 that the first and second switchably conductive devices have different threshold voltages cannot reasonably be construed as an affirmative statement that the limitation is in the Kaplinsky reference. In other words, the Applicant respectfully submits that the Examiner cannot read into the Kaplinsky reference what is not there. Accordingly, Kaplinsky does not teach or suggest the limitations "a first switchably conductive device characterized by a first threshold voltage" and "a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage" of Applicant's claim 3.

In view of the above, the Applicant respectfully submits that the rejection of claim 3 under 35 U.S.C. § 102(b) should be withdrawn.

As per claim 4, claim 4 recites the same limitations as claim 3 and adds additional limitations. For the same reasons that Kaplinsky does not meet the limitations of claim 3, Kaplinsky also does not therefore meet the limitations of claim 4. Accordingly, the Applicant respectfully submits that the rejection of claim 4 under 35 U.S.C. § 102(b) should be withdrawn.

As per claim 1, claim 1 recites similar limitations as claim 3, in method form, including "a first switchably conductive device characterized by a first threshold voltage" and "a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage". For the same reasons that Kaplinsky does not meet the limitations of claim 3, Kaplinsky also does not therefore meet the limitations of claim 1. Accordingly, the Applicant respectfully submits that the rejection of claim 1 under 35 U.S.C. § 102(b) should be withdrawn.

As per claim 2, claim 2 recites the same limitations as claim 3 and adds additional limitations. For the same reasons that Kaplinsky does not meet the limitations of claim 1, Kaplinsky also does not therefore meet the limitations of claim 2. Accordingly, the Applicant respectfully submits that the rejection of claim 2 under 35 U.S.C. § 102(b) should be withdrawn.

As per claim 7, claim 7 recites similar limitations as claim 3, including "a first switchably conductive device characterized by a first threshold voltage" and "a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage". For the same reasons that Kaplinsky does not meet the limitations of claim 3, Kaplinsky also does not therefore meet the limitations of claim 7. Accordingly, the Applicant respectfully submits that the rejection of claim 7 under 35 U.S.C. § 102(b) should be withdrawn.

As per claim 8, claim 8 recites the same limitations as claim 7 and adds additional limitations. For the same reasons that Kaplinsky does not meet the limitations of claim 7, Kaplinsky also does not therefore meet the limitations of claim 8. Accordingly, the Applicant respectfully submits that the rejection of claim 8 under 35 U.S.C. § 102(b) should be withdrawn.

b. Claims 10-11

Claim 10 recites:

> A method for controlling the slew rate of transition edges of a digital signal on a node of an integrated circuit, said method comprising the steps of:
> monitoring a level of a driving voltage;
> when said level reaches a first threshold voltage, stepping down conduction of current to said node;
> when said level reaches a next predefined threshold voltage, stepping down conduction of current to said node.

The Examiner cites Vajapey in rejecting Claims 10 and 11 under 35 U.S.C. § 102(b). In particular, the Examiner states that Vajapey teaches the steps of monitoring a level of a driving voltage (use the threshold voltages of transistors P1 and P2 as first and second threshold levels), when the level reaches a first threshold voltage, stepping down conduction of current to said node (gradually turn off the conduction of transistor P1), and when the level reaches a next predefined threshold voltage (the second threshold level), stepping down conduction of current of said node (gradually turn off the conduction of transistor P2).

The Applicant respectfully traverses the Examiner's characterization of what Vajapey fairly teaches. With regards to P1 and P2, again there is nothing to suggest in Vajapey that P1 and P2 have different threshold voltages. In col. 3, lines 62-64, the Examiner has underlined that passage stating that the "width (w) and channel length (l) of each transistor determines its current carrying capacity which affects switching time". However, the current carrying capacity is not related to the threshold voltage

of the transistor. The threshold voltage of the transistor refers to the gate-to-source voltage at which the FET device actually begins conducting current. In contrast, the current carrying capacity (saturation current) is the maximum amount of current that can flow through the channel. This occurs when the device is in the saturation region. The dimensions of the channel affect the saturation current and therefore how fast the signal will switch from one polarity to the other (i.e., the "switching time" referred to in this passage).

However, again, nowhere in the Vajapey reference is there mention that the threshold voltages of the two transistors P1 and P2 are actually different. Accordingly, per *In re Evanega*, the mere absence from the Vajapey reference of the explicit requirement of claim 10 that the first and second switchably conductive devices have different threshold voltages cannot reasonably be construed as an affirmative statement that the requirement is in the Vajapey reference. Therefore, the Applicant respectfully submits that the Examiner cannot read into the Vajapey reference what is not there.

The trigger point in Vajapey for turning on P1 and P2 in succession is a delay time. In particular, Vajapey specifically instructs in Col. 4, lines 60-63 that "the turn-on of transistor P2 is delayed for a period of time after the turn-on of transistor P1. After the voltage on output terminal 160 reaches a predetermined voltage, transistor P2 is turned on." Thus, Vajapey monitors not the level of the *driving* voltage as recited in Applicant's claim 10, but the level of the *output* voltage on line 160.

Accordingly, in view of all of the above, Vajapey does not teach or suggest the limitations "monitoring a level of a driving voltage", "when said level reaches a first threshold voltage, stepping down conduction of current to said node", "when said level reaches a next predefined threshold voltage, stepping down conduction of current to said node" of Applicant's claim 10.

The Applicant respectfully submits that the rejection of claim 10 under 35 U.S.C. § 102(b) should therefore be withdrawn.

As per claim 11, claim 11 recites the same limitations as claim 10 and adds additional limitations. For the same reasons that Vajapey does not meet the limitations of claim 10, Vajapey also does not therefore meet the limitations of claim 11. Accordingly, the Applicant respectfully submits that the rejection of claim 11 under 35 U.S.C. § 102(b) should be withdrawn.

II. Rejections of Claims Under 35 U.S.C. § 103

1. Response to Rejections of Claims Under 35 U.S.C. § 103

As per claim 5, claim 5 recites the same limitations as claim 3 and adds additional limitations. For the same reasons that Kaplinsky does not meet the limitations of claim 3, and that Vajapey does not meet the limitations of claim 10, Kaplinsky in view of Vajapey does not meet the limitations of claim 5. Accordingly, the Applicant respectfully submits that the rejection of claim 5 under 35 U.S.C. § 103(b) should be withdrawn.

As per claim 6, claim 6 recites the same limitations as claim 3 and adds additional limitations. For the same reasons that Kaplinsky does not meet the limitations of claim 3, and that Vajapey does not meet the limitations of claim 10, Kaplinsky in view of Vajapey does not meet the limitations of claim 6. Accordingly, the Applicant respectfully submits that the rejection of claim 6 under 35 U.S.C. § 103(b) should be withdrawn.

As per claim 2, claim 2 recites the same limitations as claim 1 and adds additional limitations. For the same reasons that Kaplinsky does not meet the limitations of claim 1, and that Vajapey does not meet the limitations of claim 10, Kaplinsky in view of Vajapey does not meet the limitations of claim 2. Accordingly, the Applicant respectfully submits that the rejection of claim 2 under 35 U.S.C. § 103(b) should be withdrawn.

As per claim 9, claim 9 recites the same limitations as claim 3 and adds additional limitations. For the same reasons that Kaplinsky does not meet the limitations of claim 7, and that Vajapey does not meet the limitations of claim 10, Kaplinsky in view of Vajapey does not meet the limitations of claim 9. Accordingly, the Applicant respectfully submits that the rejection of claim 9 under 35 U.S.C. § 103(b) should be withdrawn.

The application is now believed to be in condition for allowance.

CONCLUSION

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 1-11 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

April 12, 2002

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Annotated Version of the Amendments

In the Claims:

Please amend the claims as follows:

6. (Amended) An apparatus in accordance with claim [3] 5, wherein said first switchably conductive device, said second switchably conductive device, and said one or more additional switchably conductive devices each [comprises] comprises a field effect [transistors (FETs)] transistor (FET).

7. (Amended) A method for controlling the slew rate of transition edges of a digital signal on a node of an integrated circuit, said method comprising the steps of:

driving, with a driving signal, a first switchably conductive device characterized by a first threshold voltage and connected between said node and a voltage source, said first switchably conductive device responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said first threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said first threshold voltage;

driving, with said driving signal, a second switchably conductive device characterized by a second threshold voltage greater than said first threshold voltage [an] and connected between said node and said voltage source, said second switchably conductive device responsive to said driving signal to allow current conduction from said voltage source to said node when said driving signal is offset from said voltage source by a voltage substantially equal to or greater than said second threshold voltage and to disallow said current conduction when said driving signal is offset from said voltage source by a voltage less than said second threshold voltage.